

ABSTRACT

In a variable resistance memory device such as a PCRAM memory device having an array variable resistance memory cells, a process is performed to detect when the on/off resistance of each variable resistance memory cell has drifted beyond predetermined tolerance levels. When resistance drift beyond the predetermined tolerance levels is detected, at least one reset pulse is applied to the cell to return the cell to its original resistance profile. The reset pulse may be applied in the form of a "hard" write signal, a "hard" erase signal, a "soft" write signal or a "soft" erase signal as appropriate, depending on the direction of the drift and the programmed state of the cell. The "hard" write and erase signals have voltage levels which may be slightly greater in magnitude than the voltage levels of normal write and erase signals, respectively, or may have slightly longer pulse widths than those of the normal write and erase signals, or both. Similarly, the "soft" write and erase signals have voltage levels which are less than that of normal write and erase signals, or may have pulse widths which are less than that of normal write and erase signals, or both.